REMARKS

The Examiner is thanked for the thorough examination of the present application, the allowance of claims 10-13 and 17-24, and the indication that claims 8 and 9 contain allowable subject matter. The Office Action object to the Abstract. Applicant has amended the abstract herein to address and overcome the objection.

Turning to the substantive rejections, the Office Action, rejected claims 1 and 3-7 under 35 U.S.C. § 102(b) as allegedly anticipated by Nakano. (US 6,005,815).

> "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). (MPEP 2131)

In embodiments described in the present application, the leak-current limited unit 108 is connected to the array of memory cells 112 via the plurality of word lines 106, as expressly recited in the independent claim 1 and shown in Fig. 1. In other words, the leak-current limited unit 108 is connected with the plurality of word lines 106.

> 1. A memory device for burn-in test, the memory device comprising:
> ***an array of memory cells; a plurality of word lines, each word line connected to a column of the array of memory cells; and***
> ***a leak-current limited unit connected to the array of memory cells via the plurality of word lines***;
> wherein during the burn-in test, the leak-current limited unit limits the current in each word line to a predetermined word line current value and ***a word line stress voltage is provided via the leak-current limited unit to stress each column of memory cells connected to one word line.***

(*Emphasis added.*) Independent claim 1 patently defines over the cited art for at least the reason that the cited art fails to disclose the features emphasized above.

The Office Action alleges that the transistors (28 and 29) of the Nakano reference correspond to the claimed leak current limited unit. If this is the case, however, then Nakano fails to disclose the claimed leak current limited unit. In Nakano, the transistors (28 and 29) are used in a test circuit 20. According to figure 5, the gates of the P-MOS FETs (28) and (29) are connected to the TEST terminal (21). The description in column 5 line 30 to line 45 describes that a HIGH level command signal is applied to the TEST terminal (21). A burn-in test is initiated when a LOW level command signal is applied to the test terminal (21). In other words, command signals are used to switch the transistors (28 and 29) to determine whether or not to set a test. Therefore, the function of the transistors (28 and 29) is to set a test not to limit leak current, as expressly claimed by claim 1.

Moreover, even though the transistors (28 and 29) of the Nakano are used to limit a leak current, Nakano does not disclose the connection relationship between the leak current limited unit and the word lines. According to the figure 5, the transistors (28 and 29) of the Nakano are connected to a word line driver (25) not connected to word lines, as recited in claim 1.

For at least the foregoing reasons, Nakano does not disclose or suggest the above-recited features of the claimed invention. Thus, the Nakano reference does not show every element of the claimed invention. Accordingly, claim 1 is allowable over Nakano. Claims 3-7 depend from base claim 1, and further define additional technical features of the present invention. In view of the patentability of the base claim, and in further view of the additional technical features, claims 3-7 are patentable over the cited reference.

REJECTIONS UNDER 35 U.S.C. § 103

The Office Action has rejected claim 2 under 35 U.S.C. § 103 (a) as allegedly unpatentable over Nakano in view of Fujita (U.S. 5,293,340). "In order to provide a *prima facie* showing of obviousness under 35 U.S.C. § 103(a), all the claim limitations must be taught or suggested by the prior art. *See, e.g., In re Royka,* 490 F. 2d 981, 180 U.S.P.Q. 580 (CCPA 1974);" MPEP 2143.03.

As stated above, patently defines over Nakano. Moreover, the Fujita also does not disclose a leak current limited unit and the connection relationship between the leak current limited unit and the word lines. That is, even if combined, the two cited references do not teach the feature of claim 2.

In view of the patentability of its base claim, and in further view of the additional features defined in claim 2, Applicant respectfully submits that dependent claim 2 is patentable over the prior art of record.

CONCLUSION

All claims 1-13 and 17-24 are believed to be in condition for allowance, and the Examiner is respectfully requested to pass those claims to issuance. If the Examiner believes a teleconference will expedite the examination of this application, the Examiner is invited to contact the undersigned attorney at 770-933-9500.

No fee is believed to be due in connection with this Amendment and Response to Office Action. If, however, any fee is deemed to be payable, you are hereby authorized to charge any such fee to deposit account 20-0778.

Respectfully submitted ,

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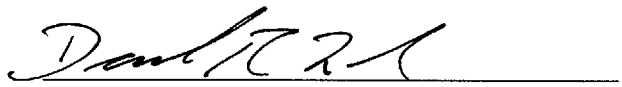
By: 

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